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EXAMINER

VINH, LAN

ART UNIT	PAPER NUMBER
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1765

DATE MAILED: 07/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,052	PRALL ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 April 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 and 21-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 21-23 is/are allowed.
- 6) ☒ Claim(s) 1-5 and 8-17 is/are rejected.
- 7) ☒ Claim(s) 6-7 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>32904</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I, claims 1-17, 21-23 in the reply filed on 4/22/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-5, 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Chiang et al (US 6,383,863)

Chiang discloses a method for forming a salicide layer. The method comprises the steps of:

forming a first conductive layer 4 and one dielectric layer on 6 the first conductive layer (col 7-14)

forming a patterned mask layer 8 over the at least one dielectric layer and overlying the first conductive layer (col 3, lines 18-20)

Art Unit: 1765

etching the dielectric layer 6 and the first conductive layer 4 using the mask as a pattern to form first and second cross-sectional sidewalls from the dielectric layer and the first conductive layer 4 (col 3, lines 20-22; fig. 2)

forming a first dielectric spacer 11 on the first sidewall and a second dielectric spacer 11 on the second sidewall, where an upper surface of each sidewall is above an upper surface of the first and second spacers (col 3, lines 37-39; fig. 4)

forming a second conductive layer over the at least one dielectric layer and over the first conductive layer (col 4, lines 25-27)

removing the second conductive layer from over the first conductive layer and leaving the second conductive layer at other locations (col 4, lines 30-35; fig. 6)

etching the at least one dielectric layer to expose the first conductive layer 4 (col 4, lines 55-60)

forming a silicide layer simultaneously on the first and second conductive layers (col 5, lines 3-9; fig. 9)

Regarding claim 2, Chiang discloses etching of the dielectric layer to expose the first conductive layer is performed in the absence of a mask (col 4, lines 55-60)

Regarding claim 3, Chiang discloses the etch of the first conductive layer defines a plurality of transistor control gates (fig. 2)

Regarding claim 4, Chiang discloses that the removal of the second conductive layer from over the first conductive layer defines a plurality of conductive plugs which contact a semiconductor wafer (col 4, lines 35-40; fig. 6)

Art Unit: 1765

Regarding claim 5, Chiang discloses the steps of forming a first silicon dioxide layer 5; forming a silicon nitride 6 on the first silicon dioxide layer; and forming a second silicon dioxide layer 10 on the silicon nitride layer (col 3, lines 10-15; fig. 3)

Regarding claim 8, Chiang discloses forming the first polysilicon layer 4 and second polysilicon layer 18 (col 3, lines 4-5; col 4, lines 36-37), forming a cobalt layer and heating the cobalt layer to form a silicide layer (col 5, lines 1-10), etching to remove the unreacted metal layer leaving a majority of the silicide layer (col 5, lines 10-15)

4. Claims 10-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Chiang et al (US 6,383,863)

Chiang discloses a method for forming a silicide layer. The method comprises the steps of:

providing a blanket polysilicon word line layer 4 and at least one dielectric layer 12 on the word line layer (fig. 1)

using a single mask, etching the word line layer and the at least one dielectric layer to define a plurality of transistor word lines (col 3, lines 19-29)

forming a blanket polysilicon plug layer over the plurality of transistor word lines and over the at least one dielectric layer (col 4, lines 25-30)

planarizing the blanket polysilicon plug layer to remove the plug layer from over the plurality of transistor word lines to form a plurality of polysilicon plugs and to expose the at least one dielectric layer 12 (col 4, lines 35-40; fig. 6)

Art Unit: 1765

subsequent to forming the plurality of polysilicon plugs, using an etch selective to polysilicon to remove the at least one dielectric layer over the plurality of transistor wordlines and to expose the plurality of transistor word lines (col 4, lines 55-60; fig. 8)

forming a self-aligned silicide layer which simultaneously forms on the plurality of transistor word lines and on the plurality of plugs (col 5, lines 5-10; fig. 9)

Regarding claim 11, Chiang discloses subsequent to etching the word line layer and the at least one dielectric layer, forming a plurality of dielectric spacers 12 on the plurality of transistor line (fig. 9, col 4, lines 49-50), forming a metal layer on the plurality of transistor lines and on the exposed portion of the spacer (col 5, lines 1-3), forming a cobalt layer and heating the cobalt layer to form a silicide layer (col 5, lines 1-10), etching to remove the unreacted metal layer leaving a majority of the silicide layer (col 5, lines 10-15)

Regarding claim 12, Chiang discloses forming a first and second sidewall from the word line and the dielectric layer (fig. 2), forming the plurality of spacers on the plurality of word lines wherein the first and second sidewall extend beyond an upper surface of the sidewall (fig. 4)

Regarding claim 13, Chiang discloses exposing the vertically oriented sidewall during the etching to remove the dielectric layer (col 3, lines 19-21)

5. Claims 15-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Chiang et al (US 6,383,863)

Art Unit: 1765

Chiang discloses a method for forming a salicide layer. The method comprises the steps of:

forming a blanket conductive transistor word line layer 4 over a semiconductor wafer substrate assembly (col 3, lines 7-9)

forming a blanket dielectric layer 5 on the transistor word line layer (fig. 1)

forming a patterned mask over the blanket dielectric layer and over the blanket conductive transistor word line layer (col 3, lines 19-21)

patterning the blanket dielectric layer and the blanket conductive transistor word line layer using the patterned mask to form a patterned dielectric layer from the blanket dielectric layer and a plurality of transistor word lines from the blanket conductive word line layer (col 3, lines 21-25; fig. 2)

forming a blanket conductive plug layer over the patterned dielectric layer, over the transistor word lines, and between adjacent transistor word lines (col 4, lines 25-30)

removing a portion of the blanket conductive plug layer by planarizing the conductive plug layer in the absence of a mask layer to form a plurality of conductive plugs (col 4, lines 35-40)

subsequent to planarizing the blanket conductive plug layer, removing the patterned dielectric layer in the absence of a mask layer to expose the plurality of transistor word lines (col 4, lines 58-60)

subsequent to removing the patterned dielectric layer, forming a blanket metal layer on the plurality of conductive plugs, the plurality of transistor word lines, and on exposed dielectric layers (col 5, lines 1-4)

Art Unit: 1765

forming a cobalt layer and heating the cobalt layer to form/to convert the cobalt layer to a silicide layer/enhancement layer while the metal on the exposed dielectric remained unreacted/unconverted (col 5, lines 1-13),

etching to remove the unreacted metal layer leaving a majority of the silicide/enhancement layer (col 5, lines 10-15)

Regarding claim 16, Chiang discloses forming a first silicon dioxide layer 5; forming a silicon nitride 6 on the first silicon dioxide layer; and forming a second silicon dioxide layer 10 on the silicon nitride layer (col 3, lines 10-15; fig. 3)

Regarding claim 17, Chiang discloses forming first and second dielectric spacers on the patterned dielectric layer and on the transistor word lines such that an inside surface of each spacer contacts the patterned dielectric layer, and wherein the patterned dielectric layer extends above a top of each of the first and second dielectric spacers (fig. 4), exposing the inside surface of each of the first and second spacers during the removal of the patterned dielectric layer (fig. 8), during the formation of the blanket metal layer, forming the blanket metal layer on the inside surface of each of the first and second spacers and removing the metal layer from the inside surface of each of the first and second spacers during the removal of the unconverted portion of the metal layer in the absence of the mask (col 5, lines 1-15)

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 1765

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 9, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al (US 6,383,863) in view of Shin et al (US 6,635,536)

Chiang method has been described above. Unlike the instant claimed inventions as per claims 9, 14, Chiang fails to disclose forming the spacer from aluminum oxide

Shin, in a method for manufacturing semiconductor device, discloses forming a spacer of SiN or aluminum oxide (col 2, lines 33-35)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Chiang method by forming the spacer from aluminum oxide because according to Shin, the spacer on a transistor can be formed of SiN or aluminum oxide film (col 2, lines 8-35)

Allowable Subject Matter

8. Claims 6-7 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Regarding claims 6-7, the cited prior art of record fails to disclose a method for forming a semiconductor device comprises the step of forming a first silicon dioxide layer wherein an upper surface of the first silicon dioxide layer is above the upper surface of the first and second spacers/ wherein an upper surface of the first silicon

Art Unit: 1765

dioxide layer is below the upper surface of the first and second spacers and an upper surface of the SIN layer is above the upper surface of the first and second spacer, in combination with the rest of the limitations of claims 6-7. The closest cited prior art of Chiang et al (US 6,383,863) discloses the step of forming a first silicon dioxide layer 5 wherein an upper surface of the first silicon dioxide layer 5 is below the upper surface of the first and second spacers 11/ wherein an upper surface of the first silicon dioxide layer is below the upper surface of the first and second spacers and an upper surface of the SIN 6 layer is below the upper surface of the first and second spacer (fig. 4)

Claims 21-23 allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claim 21, the cited prior art of record fails to disclose a method for forming a semiconductor device comprises the step of forming a first silicon nitride spacer along the first sidewall of the at least one polysilicon transistor control gate and a second silicon nitride spacer along the second sidewall of the at least one polysilicon transistor control gate, wherein an upper surface of each spacer extends above the upper surface of the polysilicon transistor control gate but does not extend above the upper surface of the silicon dioxide buffer layer. The closest cited prior art of Chiang et al (US 6,383,863) discloses the steps of forming a first silicon nitride spacer 11 along the first sidewall of the at least one polysilicon transistor control gate and a second silicon nitride spacer along the second sidewall of the at least one polysilicon transistor control gate, wherein an upper surface of each spacer 11 extends above the upper

Art Unit: 1765

surface of the polysilicon transistor control gate and above the upper surface of the silicon dioxide buffer layer 5 (fig. 4)

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471.

The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



LV
July 5, 2005